500-kHz Push-Pull DC-DC Converter With Integrated Secondary Synchronous Rectification Control

FEATURES

- 12-V to 72-V Input Voltage Range
- Compatible with ETSI 300 132-2 100 V, 100-ms Transients
- Integrated Push-Pull 1-A Primary Drivers
- Voltage Mode Control
- Voltage Feedforward Compensation
- High Voltage Pre-Regulator Operates During Start-Up
- Current Sensing On OUT_B Primary Device

- Hiccup Current Control During Shorted Load
- Low Input Voltage Detection
- Programmable Soft-Start Function
- Programmable Oscillator Frequency
- Over Temperature Protection

APPLICATIONS

- Network Cards
- Power Supply Modules

DESCRIPTION

Si9124 is a dedicated push-pull controller IC ideally suited to fixed telecom dc-dc converter applications where high efficiency is required at low output voltages (e.g. <3.3 V). Designed to operate within the voltage range of 12-72 V and withstand 100 V, 100 ms transients, the IC is capable of controlling and directly driving both primary side MOSFET switches of a push-pull circuit.

High conversion efficiency is achieved by use of synchronous rectifying MOSFET transistors in the secondary. Due to the very low on-resistance of the secondary MOSFETs, a significant increase in the efficiency can be achieved as compared with conventional Schottky diodes for today's low output voltages. On-chip control of the dead time delays between the primary and secondary signals keep efficiencies high and prevents accidental destruction of the power transformer or wasted energy from self timed approaches. Such a system can achieve conversion efficiencies well in excess of 90%.
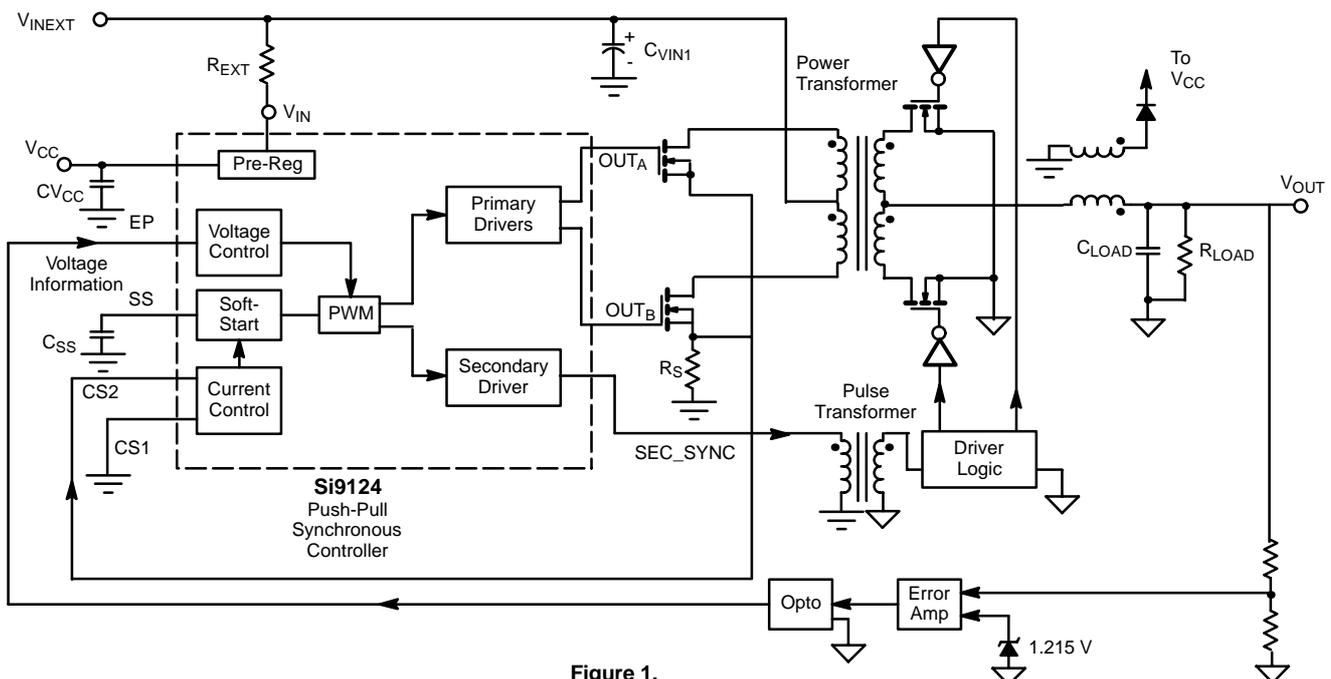
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

Si9124

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DESCRIPTION (CONTINUED)

Si9124 has advanced current monitoring circuitry to permit the user to set the maximum current in the primary circuit. Such a feature acts as protection against output shorts. Upon sensing an overload condition, the converter is shut off for a period of time and then soft-start cycle is re-initiated, achieving hiccup mode operation. Current sensing is by means of a sense resistor on the primary device. An integrated over-temperature shutdown circuit also protects the system.

The 100-V depletion mode MOSFET integrated pre-regulator

circuit permits direct operation from input voltage with only one series resistor during startup. The pre-regulator automatically disconnects from the input supply when the output voltage is established by means of a feedback winding from the filter inductor.

Si9124 is available in TSSOP-16 pin package. In order to satisfy the stringent ambient temperature requirements, Si9124 is rated to handle the industrial temperature range of −40 to 85°C.
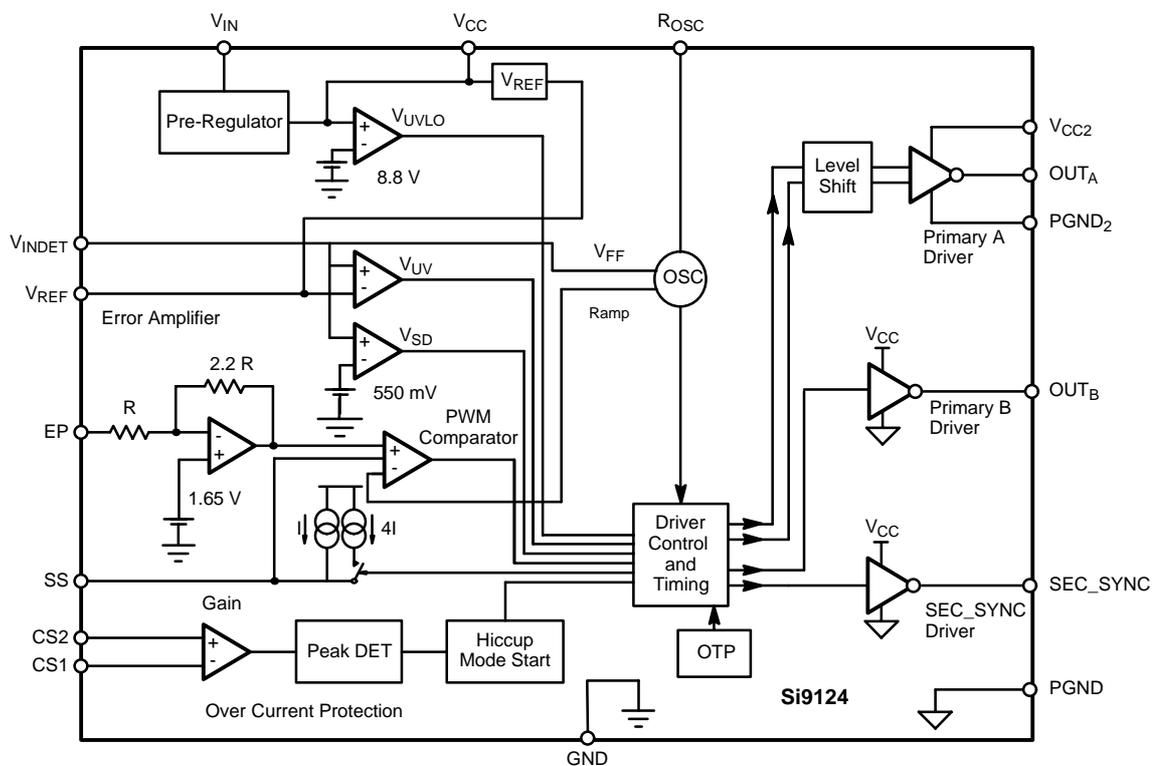
DETAILED BLOCK DIAGRAM

Figure 2.

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ABSOLUTE MAXIMUM RATINGS (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{IN} (Continuous) . . . . 75 V

V_{IN} (100 ms) . . . . 100 V

V_{CC} . . . . 14.5 V

V_{CC2} . . . . 14.5 V

V_{REF}, R_{OSC} . . . . -0.3 V to V_{CC} + 0.3 V

Logic Inputs . . . . -0.3 V to V_{CC} + 0.3 V

Analog Inputs . . . . -0.3 V to V_{CC} + 0.3 V

SEC_SYNC Drive Current . . . . 35 mA

HV Pre-Regulator Input Current (continuous) . . . . 5 mA

Storage Temperature . . . . -65 to 150°C

Operating Junction Temperature . . . . 125°C

Power Dissipation[a]

TSSOP-16 (T_A = 25°C) . . . . 1.25 W

Thermal Impedance (Θ_{JA})

TSSOP-16[b] . . . . 100°C/W

Notes

a. Device mounted on JEDEC compliant 1S2P (4 layer) test board.

b. Derate -10 mW/°C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{IN} . . . . 36 to 72 V

$C_{VIN1} \parallel C_{VIN2}$ . . . . 100 µF/ESR ≤ 100 mΩ and 0.1 µF

V_{CC} Operating . . . . 10 to 13.2 V

CV_{CC} . . . . 4.7 µF

f_{OSC} . . . . 200 to 600 kHz

R_{OSC} . . . . 24 to 72 kΩ

R_{EXT} . . . . 1.4 kΩ

C_{SS} . . . . 22 nF

C_{REF} . . . . 1.0 µF

C_{BOOST} . . . . 0.1 µF

C_{LOAD} . . . . 150 µF

Analog Inputs . . . . 0 to V_{CC} -0.3 V

Digital Inputs . . . . 0 to V_{CC}

Reference Voltage Output Current . . . . 0 to 2.5 mA

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified CS1 = CS2 = 0 V, f_{NOM} = 500 kHz, V_{IN} = 48 V V_{INDET} = 4.8 V; 10 V ≤ V_{CC} ≤ 13.2 V, $V_{CC2} = V_{CC}$	Limits -40 to 85°C			Unit
			Min[b]	Typ[c]	Max[b]	
Reference (3.3 V)						
Output Voltage	V_{REF}	V_{CC} = 12 V, 25°C Load = 0 mA	3.2	3.3	3.4	V
Short Circuit Current	I_{SREF}	V_{REF} = 0 V			-50	mA
Load Regulation	dVr/dlr	I_{REF} = 0 to -2.5 mA		-30	-75	mV
Power Supply Rejection	PSRR	@ 100Hz		60		dB
Oscillator						
Accuracy (1% R_{OSC})		R_{OSC} = 30 kΩ, f_{NOM} = 500 kHz	-20		20	%
Max Frequency	F_{MAX}	R_{OSC} = 24 kΩ		600		kHz
Error Amplifier						
Input Bias Current	I_{BIAS}	V_{EP} = 0 V	-40		-15	µA
Gain	A_V			-2.2		V/V
Bandwidth	BW			5		MHz
Power Supply Rejection	PSRR	@ 100Hz		60		dB
Slew Rate	SR			0.5		V/µs
Current Sense Amplifier						
Input Voltage CM Range	V_{CM}	V_{CS1} - GND, V_{CS2} - GND		±150		mV
Input Amplifier Gain	A_{VOL}			17.5		dB
Input Amplifier Bandwidth	BW			5		MHz
Input Amplifier Offset Voltage	V_{OS}			±5		mV
V_{CC} Hiccup Threshold	V_{THCUP}	Increase CS2 Until SS Hiccups		150		mV
Hysteresis		Decrease CS2 Until SS Clamps		-50		

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SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified $CS1 = CS2 = 0$ V, $f_{NOM} = 500$ kHz, $V_{IN} = 48$ V $V_{INDET} = 4.8$ V; 10 V $\leq V_{CC} \leq 13.2$ V, $V_{CC2} = V_{CC}$		Limits -40 to 85°C			Unit
				Min[b]	Typ[c]	Max[b]	
PWM Operation							
Duty Cycle[e]	D_{MAX}	$f_{OSC} = 500$ kHz	$V_{EP} = 0$ V	90	92	95	%
	D_{MIN}		$V_{EP} = 1.85$ V		< 15		
Pre-Regulator							
Input Voltage (Continuous)	V_{IN}	$I_{IN} = 10$ μA				72	V
Input Leakage Current	I_{LKG}	$V_{IN} = 72$ V, $V_{CC} > V_{REG}$				10	μA
Regulator Bias Current	I_{REG1}	$V_{IN} = 72$ V, $V_{INDET} < V_{SD}$			86	200	
	I_{REG2}	$V_{IN} = 72$ V, $V_{INDET} > V_{REF}$			4.5	7.5	mA
Pre-Regulator Drive Capacility	I_{START}	$V_{CC} < V_{REG}$		20			
V_{CC} Pre-Regulator Turn Off Threshold Voltage	V_{REG1}	$V_{INDET} > V_{REF}$		7.4	9.1	10.4	
			$T_A = 25°C$	8.5	9.1	9.7	
	V_{REG2}	$V_{INDET} = 0$ V			9.2		V
Undervoltage Lockout[d]	V_{UVLO}	V_{CC} Rising		7.15	8.6	9.8	
			$T_A = 25°C$	8.1	8.6	9.3	
V_{UVLO} Hysteresis	$V_{UVLOHYS}$				0.5		
Soft-Start							
Soft-Start Current Output	I_{SS1}	$0 < V_{SS} < 2\,V_{be}$		12	20	28	μA
	I_{SS2}	$2\,V_{be} < V_{SS} < 4.8$ V		60	100	200	
Soft-Start Completion Voltage	V_{SS_COMP}	Normal Operation		7.35	8.1	8.85	V
Shutdown							
V_{INDET} Shutdown FN	V_{SD}	V_{INDET} Rising		350	550	720	mV
V_{INDET} Hysteresis		V_{INDET}			200		
V_{INDET} Input Threshold Voltages							
V_{INDET} - V_{IN} Under Voltage	V_{UV}	V_{INDET} Rising		3.13	3.3	3.46	V
V_{INDET} Hysteresis		V_{INDET}			0.3		
Over Temperature Protection							
Activating Temperature		T_J Increasing			160		°C
De-Activating Temperature		T_J Decreasing			130		
Converter Supply Current (V_{CC})							
Shutdown	I_{CC1}	Shutdown, $V_{INDET} = 0$ V		50	140	350	μA
Switching Disabled	I_{CC2}	$V_{INDET} < V_{REF}$		1.8	2.8	3.8	
Switching w/o Load[f]	I_{CC3}	$V_{INDET} > V_{REF}$, $f_{NOM} = 500$ kHz		3.0	4.4	6.8	
Switching with C_{LOAD}	I_{CC4}	$V_{CC} = 12$ V, $OUT_A = OUT_B = 3$ nF, $C_{SEC\_SYNC} = 0.3$ nF			15.2		mA
V_{CC} Hiccup Current	I_{HCUP}	$CS2 - CS1 = 200$ mV, $C_{OUTA} = C_{OUTB} = 3$ nF $C_{SEC\_SYNC} = 0.3$ nF			4.3		

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified CS1 = CS2 = 0 V, f_{NOM} = 500 kHz, V_{IN} = 48 V V_{INDET} = 4.8 V; 10 V ≤ V_{CC} ≤ 13.2 V, V_{CC2} = V_{CC}	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Output A Primary Driver						
Output High Voltage	V_{OH}	Sourcing 10 mA	V_{CC2} - 0.3			V
Output Low Voltage	V_{OL}	Sinking 10 mA			$PGND_2$ + 0.3	
V_{CC2} Current	I_{CC5}	V_{CC2} = 12 V, $PGND_2$ = 0 V	0.1	1.55	1.1	mA
Peak Output Source	I_{SOURCE}			-1.0	-0.75	A
Peak Output Sink	I_{SINK}		0.75	1.0		
Rise Time	t_r	T_A = 25°C, C_{OUTA} = 3 nF, V_{CC} = 12 V, 20 - 80%		18	28	ns
Fall Time	t_f			22	28	
Output B Primary Driver						
Output High Voltage	V_{OH}	Sourcing 10 mA	V_{CC} - 0.3			V
Output Low Voltage	V_{OL}	Sinking 10 mA			0.3	
Peak Output Source	I_{SOURCE}	V_{CC} = 12 V, PGND = 0 V		-1.0	-0.75	A
Peak Output Sink	I_{SINK}		0.75	1.0		
Rise Time	t_r	T_A = 25°C, C_{OUTB} = 3 nF, V_{CC} = 12 V, 20 - 80%		19	28	ns
Fall Time	t_f			24	28	
Secondary_Synchronous Driver						
Output High Voltage	V_{OH}	Sourcing 10 mA	V_{CC} - 0.4			V
Output Low Voltage	V_{OL}	Sinking 10 mA			0.4	
Leading Edge Delays	t_{d1}	T_A = 25°C, V_{CC} = 12 V, L_X = 48 V, See Figure 3		80	110	ns
	t_{d3}			80	110	
Trailing Edge Delays	t_{d2}	C_{OUTA} = C_{OUTB} = 3nF, C_{SEC_SYNC} = 0.3 nF		80	110	
	t_{d4}			80	110	
Peak Output Source	I_{SOURCE}	V_{CC} = 12 V		-100		mA
Peak Output Sink	I_{SINK}			100		
Rise Time	t_r	T_A = 25°C, C_{SEC_SYNC} = 0.3 nF, V_{CC} = 12 V, 20 - 80%		16	28	ns
Fall Time	t_f			17	28	
Voltage Mode						
Error Amplifier	t_{d1A}	Input to A-side switch off		<200		ns
	t_{d2B}	Input to B-side switch off		<200		
Current Mode						
Current Amplifier	t_{d3A}	Input to A-side switch off		<200		ns
	t_{d4B}	Input to B-side switch off		<200		

Notes
a.   Refer to PROCESS OPTION FLOWCHART for additional information.
b.   The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (-40° to 85°C).
c.   Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at V_{CC} = 12 V unless otherwise noted.
d. V_{UVLO} tracks V_{REG1} by a diode drop.
e.   Measured on OUT_A or OUT_B outputs.
f.   Note total supply current drawn is I_{CC3} plus I_{CC5}.
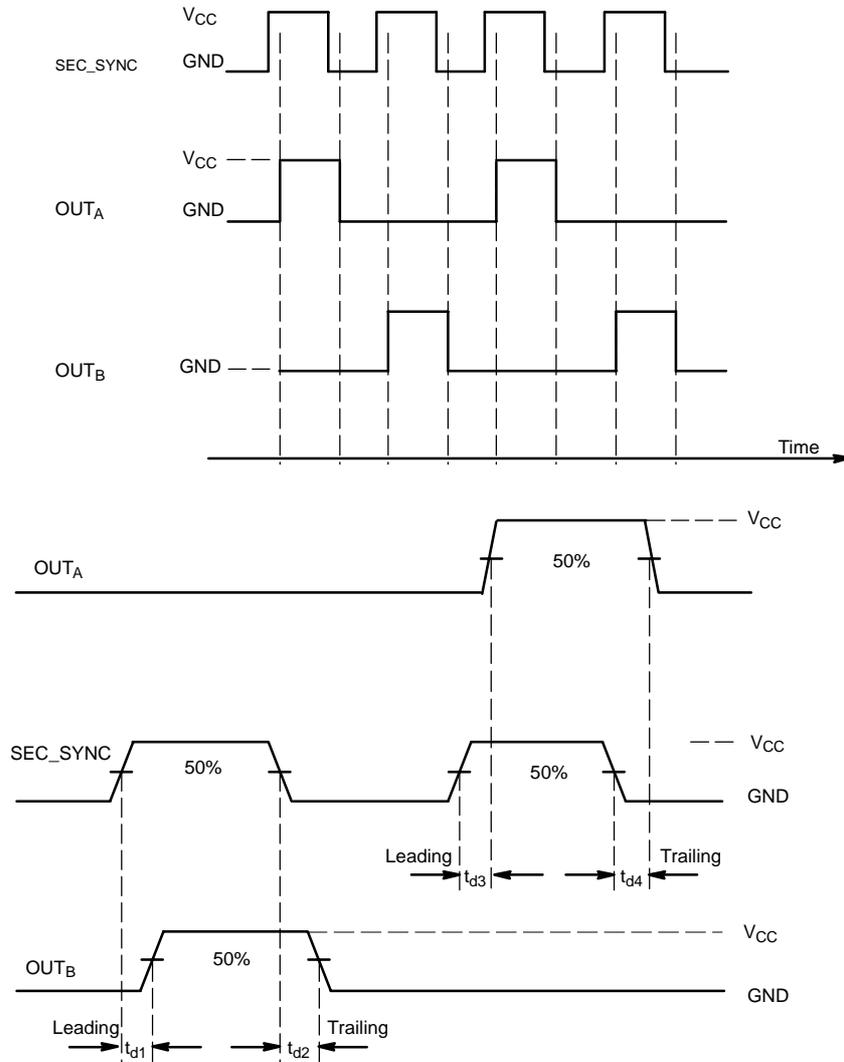
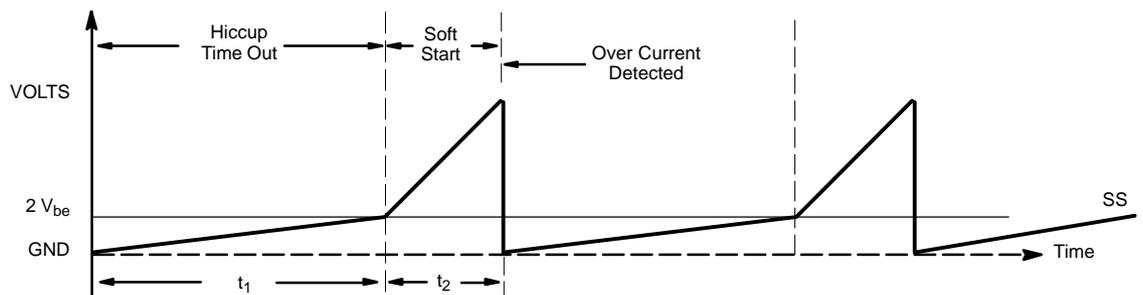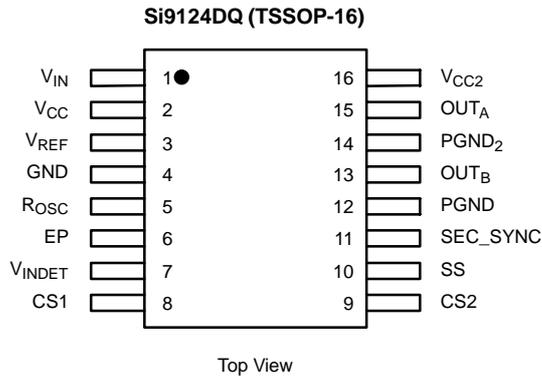## TIMING DIAGRAMS FOR MOS DRIVERS

Figure 3.

Figure 4. Soft-Start, Hiccup Mode Operation

PIN CONFIGURATION

Si9124DQ (TSSOP-16)

V_{IN}	1●	16	V_{CC2}
V_{CC}	2	15	OUT_A
V_{REF}	3	14	$PGND_2$
GND	4	13	OUT_B
R_{OSC}	5	12	PGND
EP	6	11	SEC_SYNC
V_{INDET}	7	10	SS
CS1	8	9	CS2

Top View

ORDERING INFORMATION

Part Number	Temperature Range	Package
Si9124DQ-T1	- 40 to 85°C	Tape and Reel
Si9124DQ		Bulk

PIN DESCRIPTION

Pin Number	Name	Function
1	V_{IN}	Input supply voltage for the start-up circuit.
2	V_{CC}	Supply voltage for internal circuitry
3	V_{REF}	3.3-V reference, decoupled with 1-μF capacitor
4	GND	Analog Ground
5	R_{OSC}	External resistor connection to oscillator
6	EP	Voltage control input
7	V_{INDET}	V_{IN} under voltage detect and shutdown function input. Shuts down or disables switching when V_{INDET} falls below preset threshold voltages and provides the feed forward voltage.
8	CS1	Current limit amplifier negative input
9	CS2	Current limit amplifier positive input
10	SS	Soft-Start control - external capacitor connection
11	SEC_SYNC	Secondary side timing signal
12	PGND	A driver power ground.
13	OUT_B	B gate drive signal – primary
14	$PGND_2$	B driver power ground
15	OUT_A	A gate drive signal – primary
16	V_{CC2}	V_{CC2} connect to V_{CC}

DETAILED FUNCTIONAL BLOCK DIAGRAM
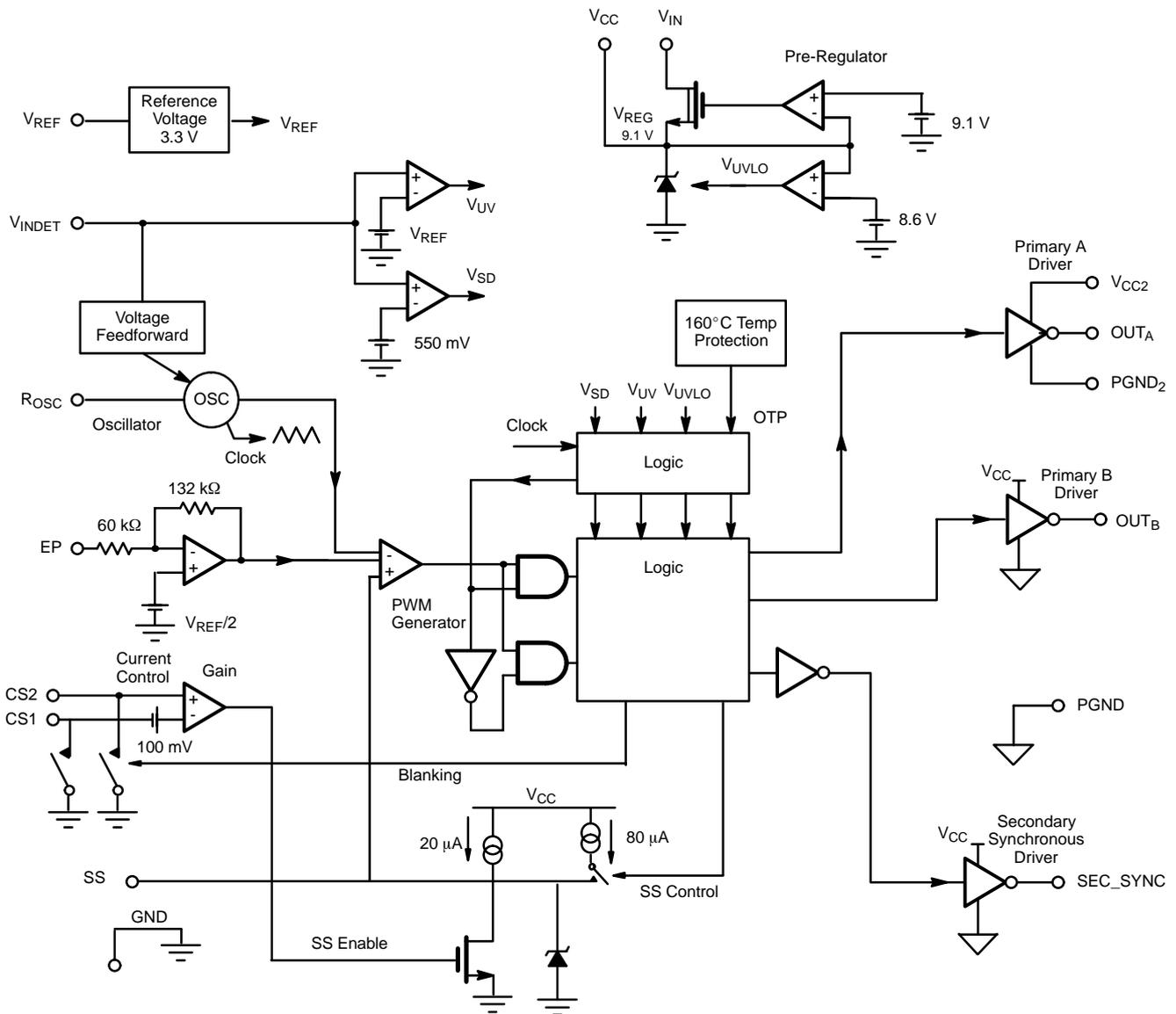
Figure 5.

DETAILED OPERATION

Start-Up

A detailed Functional Block Diagram is shown in [Figure 5](#) with additional detail of the pre-regulator shown in [Figure 6](#). The pre-regulator circuit acts as a linear regulator to provide V_{CC} directly from the V_{INEXT} supply until the V_{CC} supply voltage between 10 V to 13.2 V can be sustained from an auxiliary winding from the secondary of the power inductor.

When V_{INEXT} rises above 0 V (see Figure 6), the internal pre-regulator begins charging the external capacitor on V_{CC}. The charging current is limited to typically 40 mA by the internal DMOS device. When Vcc exceeds the UVLO voltage of 8.8 V, a soft-start cycle of the controller is initiated to provide power to the secondary. Once switching commences, the internal gate drivers for the primary side switching transistors and the drive current into the secondary synchronization driver draw additional current from the V_{CC} capacitor and pre-regulator.

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The pre-regulator will remain on until V_{CC} equals V_{REG} but between V_{UVLO} and V_{REG}, excessive current may result in V_{CC} falling below V_{UVLO} and stopping soft start operation. This situation is avoided by the hysteresis between V_{REG} and V_{UVLO} and correct sizing of the V_{CC} capacitor, bootstrap capacitor, the soft-start capacitor, the primary MOSFET gate driving charge, and load on the SEC_SYNC output. The value of the V_{CC} capacitor should be chosen to be capable of maintaining soft start operation with V_{CC} above V_{UVLO} until the V_{CC} current can be supplied from the external circuit (e.g. via an auxiliary winding on the secondary inductor).
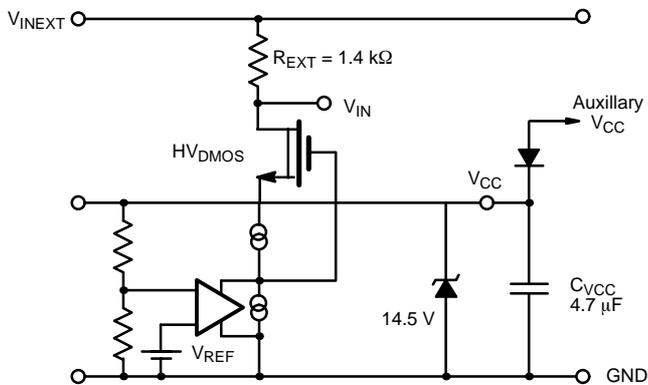
Figure 6. High-Voltage Pre-Regulator Circuit

The feedback voltage from the output of the auxiliary winding must sustain V_{CC} above V_{REG} to fully disconnect the pre-regulator, isolating V_{CC} from V_{INEXT}. V_{CC} is then maintained above V_{REG} for the duration of operation. In the event of an over voltage condition on V_{CC}, an internal voltage clamp turns on at 14.5 V to shunt excessive current to GND. In systems where operation is directly from a 12 V supply, V_{INEXT} and V_{CC} can be connected to the 12 V bus.

The soft-start circuit is designed for the dc-dc converter to start up in an orderly manner and reduce component stress. Soft start is achieved by ramping the maximum achievable duty cycle during the soft start time. The duty cycle is increased from zero to the final value at the rate set by the an external capacitor, C_{SS} as shown in Figure 7. The hiccup time is set by an internal 20 µA current source charging C_{SS} from 0 V to 2 V_{be}, at which point switching begins. Then a 100 µA charging current is applied to C_{SS} to charge from 2 V_{be} to the final value controlling the duty cycle as it rises. In the event of UVLO, shutdown or over current, the SS pin will be held low (< 1 V) disabling driver switching. A longer soft-start time may be needed for highly capacitive loads and high peak-output current applications. In the event of an over current condition being detected, the soft-start pin will be pulled low and the cycle will start again performing a hiccup as shown in Figure 4. The hiccup off-time, t_1, is given by:

$$t_1 \approx C_{SS} \times \frac{1.2\text{ V}}{20\text{ µA}}$$

The soft-start time t_2 is can be estimated as:

$$t_2 \approx \frac{\left(C_{SS} \times V_{OUT} \times n\right)}{\left(K \times 100\text{ µA}\right)}$$

where V_{OUT} is the output of the converter, and n is the turns ratio of the primary to each secondary winding, and K is the ratio of the resistive divider from V_{INEXT} to V_{INDET} (typically 10/1).
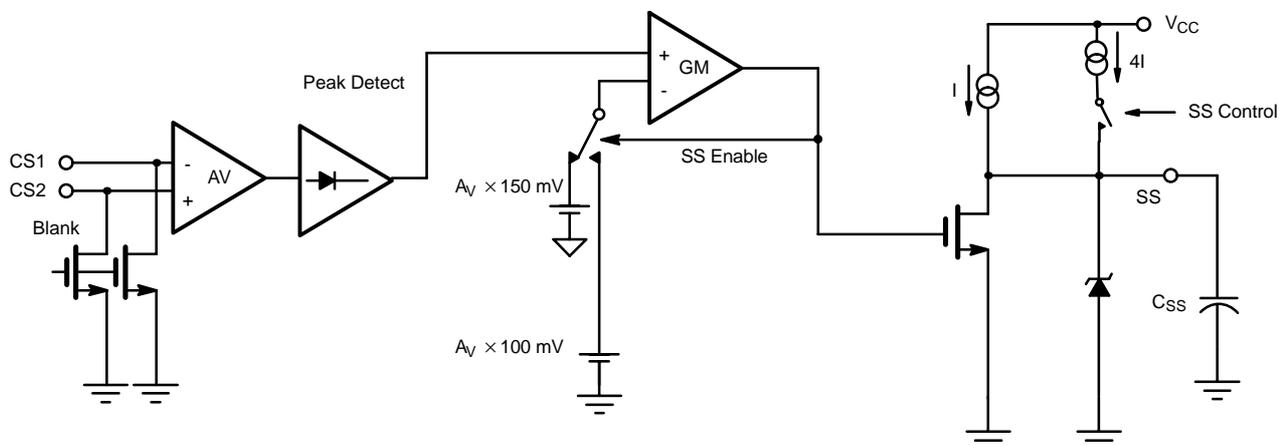

Figure 7. Current-Sense and Soft-Start Circuit Block Diagram

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Care should be taken to control the operating time using the internal preregulator to prevent excessive power dissipation in the IC. The use of an external dropping resistor connected in series with the V_{IN} pin to drop the voltage during start up is recommended. The value of R_{EXT} is selected to drop the input voltage to the IC under worst case conditions thereby dissipating power in the resistor, instead of the IC. If the supply output is shorted and the auxiliary winding does not provide the V_{CC} current, then continuous soft start cycles will occur. The average power in the IC during start-up where the hiccup operation would be performed continuously is given by:

$$\text{Power (IC)} = V_{IN} \times \frac{\left[t_1 I_{CC2} + t_2 \left(I_{CC4} + I_{CC5} + I_{SEC\_SYNC} \right) \right]}{(t_1 + t_2)}$$

$$\text{Power} \left(R_{EXT} \right) = V_{ID} \times \frac{\left[t_1 I_{CC2} + t_2 \left(I_{CC4} + I_{CC5} + I_{SEC\_SYNC} \right) \right]}{(t_1 + t_2)}$$

$$\text{where } V_{ID} = \left(V_{INEXT} - V_{IN} \right)$$

where I_{CC2} is the non-switching supply current, I_{CC4} and I_{CC5} are the supply current while switching, and I_{SEC_SYNC} is the average current out of the SEC_SYNC pin, and t_1 and t_2 are defined in Figure 4.

After the feedback voltage from the secondary overrides the internal pre-regulator, no current flows through R_{EXT}. An example of the feedback circuitry is shown in Figure 15.

The SS pin has a predictable $+1.25\text{-mV}/^\circ\text{C}$ temperature coefficient and can be used to continuously monitor the junction temperature of the IC for a given power dissipation.

Reference

The reference voltage of Si9124 is set at 3.3 V. The reference voltage should be de-coupled externally with a 0.1 μF capacitor. The V_{REF} voltage is 0 V in shutdown mode and has 50-mA source capability.

Voltage Mode PWM Operation

Under normal load conditions, the IC operates in voltage mode and generates a fixed frequency pulse-width modulated signal to the drivers. Duty cycle is controlled over a wide range to maintain the output voltage under line and load variation. Voltage feed-forward is also included to improve line regulation and transient response. In the push-pull topology requiring isolation between output and input, the reference voltage and error amplifier must be supplied externally, usually on the secondary side.

The error information is usually passed to the power controller through an opto-coupling device for isolation. The error information enters the IC via pin EP and where 0 V results in the maximum duty cycle, whilst 2 V represents minimum duty cycle. The EP error signal is gained up by -2.2X via an inverting amplifier and compared against the internal ramp generator. The relationship between Duty Cycle and V_{EP} is shown in the Typical Characteristic section, Duty Cycle vs. V_{EP} at 25 $^\circ$C , page 12.

Voltage feed-forward is implemented by taking the attenuated V_{INEXT} signal at V_{INDET} to directly modulate he duty cycle. This relationship is shown in the Typical Characteristic section, Duty Cycle vs. V_{INDET}, page 12. The response time to line transients is very short since the PWM duty cycle is charged directly without having to go through the error amplifier feedback loop. At start-up, i.e., once V_{CC} is greater than V_{UVLO}, switching is initiated under soft-start control which increases maximum attainable switch on-time linearly over the soft-start period. Start-up from a V_{INDET} power down, over-temperature, or over current is also initiated under soft-start control.

Push-Pull and Synchronous Rectification Timing Sequence

The PWM signal generated within the IC controls the OUT_A and OUT_B drivers on alternate cycles. A period of inactivity always results after initiation of the soft-start cycle until the soft-start voltage reaches approximately 2 V_{be} and PWM generated switching begins. The timing and coordination of the drives to the primary and secondary stages is very important and the relationships are shown in Figure 3. It is essential to avoid the situation where both of the secondary MOSFETs are on when either the OUT_A or OUT_B switches are active. In this situation the transformer would effectively be presented with a short across the output. To avoid this a timing signal is made available which is ahead of the primary drive outputs by 80 ns.

Primary MOSFET Drivers

The drive voltage for the primary MOSFETs is provided directly from the V_{CC} and V_{CC2} supply. The switch gate drive signals OUT_A and OUT_B are shown in Figure 3. The drive currents for the primary side MOSFETs is supplied from the V_{CC} and V_{CC2} supply and can influence start up conditions.

Secondary Synchronization Driver

The secondary side MOSFETs are driven by the SEC_SYNC output via a pulse transformer and gate driver circuits. The time relationships are shown in Figure 3. Logic circuitry on the secondary side is required to align the synchronous rectifier gate drive with the primary drive. The current supplied to the pulse transformer is drawn from V_{CC}.

Oscillator

The oscillator is designed to operate at a frequencies up to 500 kHz. The 500-kHz operating frequency allows the converter to minimize the inductor and capacitor size, improving the power density of the converter. The oscillator and therefore switching frequency is programmable by a resistor on the R_{OSC} pin. The relationship is shown in the Typical Characteristics, F_{OSC} vs. R_{OSC}.

Hiccup Operation

Current limiting is achieved by monitoring the differential voltage between CS1 and CS2 pins which are connected across a primary sense resistor. Once the differential voltage exceeds the 150-mV trigger point, Hiccup operation is started. The soft-start voltage on the SS pin is pulled to ground and switching stops until the SS pin charges up to 2 V_{be} whereupon a duty cycle limited soft start is initiated. The upper and lower switching points of the current limit have 50 mV of hysteresis.

V_{INEXT} Voltage Monitor – V_{INDET}

The Si9124 provides a means of sensing the voltage on V_{INEXT} to control the operating mode and provides the feed-forward control voltage to the PWM controller. This is

achieved by choosing an appropriate resistive tap between V_{INEXT} and ground.

When the V_{INDET} voltage is greater than 720 mV but less than V_{REF} and V_{CC} is greater than V_{UVLO}, all internal circuitry is enabled, but switching is stopped.

V_{INDET} also provides the input to the voltage feed-forward function by adjusting the amplitude of the PWM ramp to the PWM comparator.
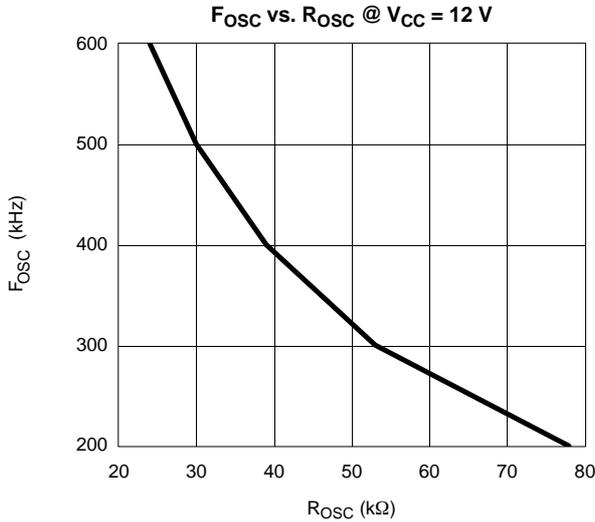
Shutdown Mode

If V_{INDET} pin is forced below 470 mV the device will enter SHUTDOWN mode. This powers down all unnecessary functions of the controller, ensures that the primary switches are off and results in a low level current demand of 150 μA from the V_{INEXT} or V_{CC} supplies.
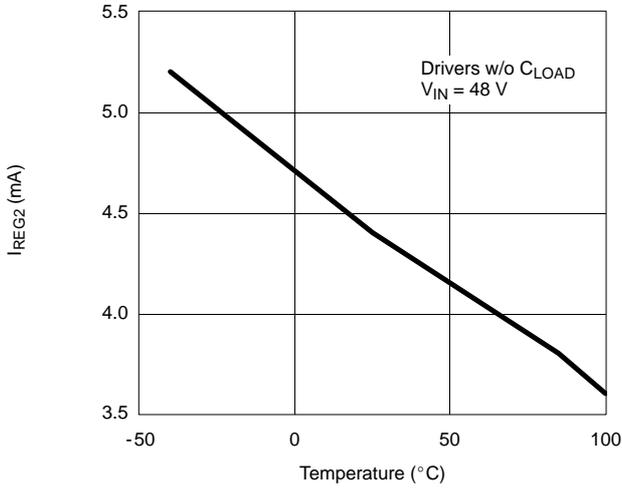
TYPICAL CHARACTERISTICS

V_{SS} vs. Temperature, V_{CC} = 12 V

V_{REG} vs. Temperature, V_{IN} = 48 V

I_{SS1} vs. V_{CC} vs. Temperature

I_{SS2} vs. V_{CC} vs. Temperature

TYPICAL CHARACTERISTICS

F_{OSC} vs. R_{OSC} @ V_{CC} = 12 V

V_{REF} vs. Temperature, V_{CC} = 12 V

I_{HCUP} vs. SS Duty Cycle, C_{SS} 22 = nF

V_{CC} = 12 V
V_{iINDET} = 4.8 V
OUT_A = OUT_B = 3 nF
C_{SEC_SYNC} = 0.3 nF

OUT_A, OUT_B Duty Cycle vs. V_{EP}

OUT_A, OUT_B Delay vs. Temperture

**Duty Cycle vs. V_{INDET} @ 25°C
V_{EP} = 1.2 V, V_{CC} = 9.5 V**
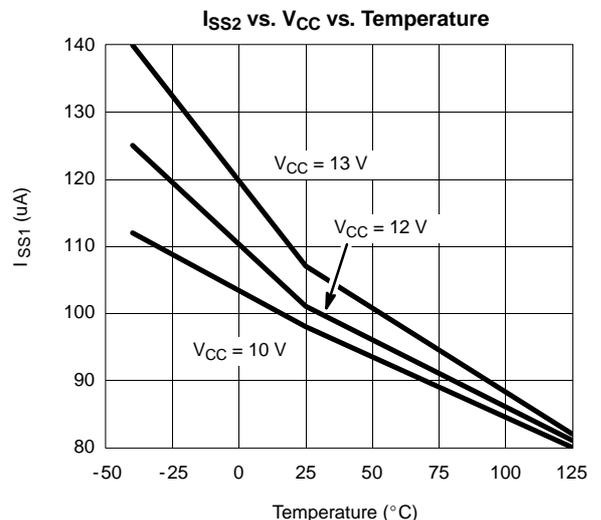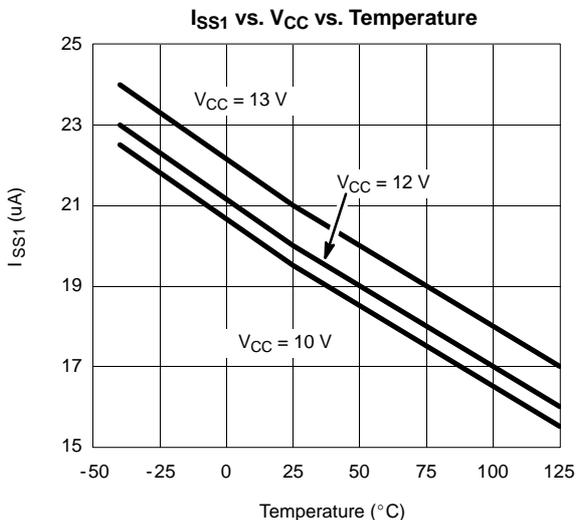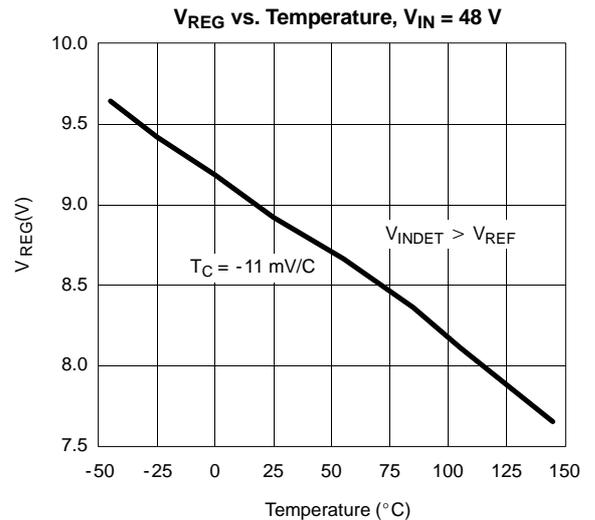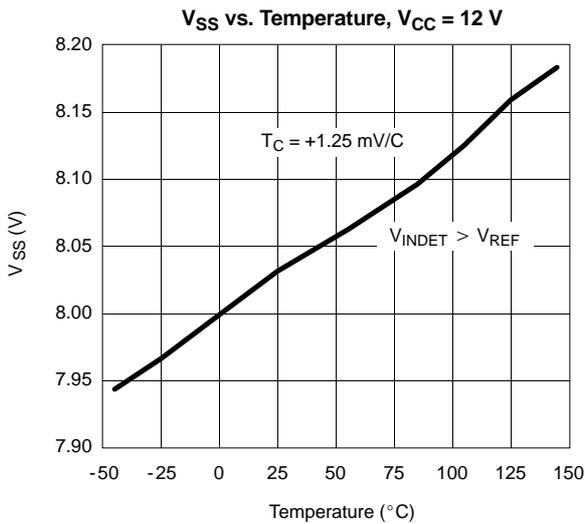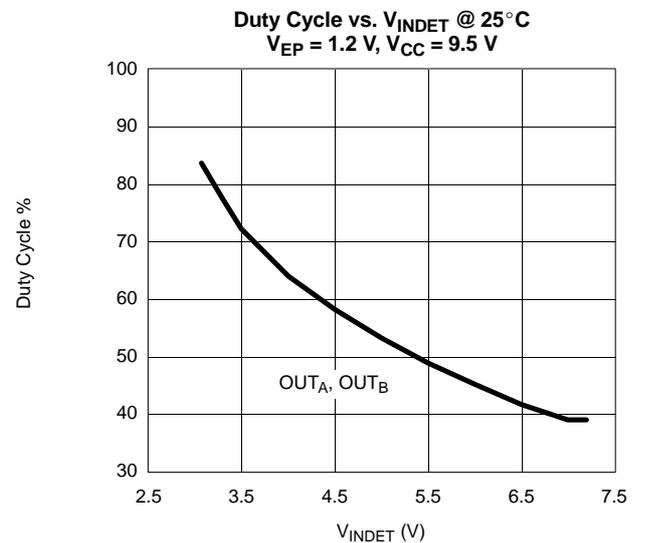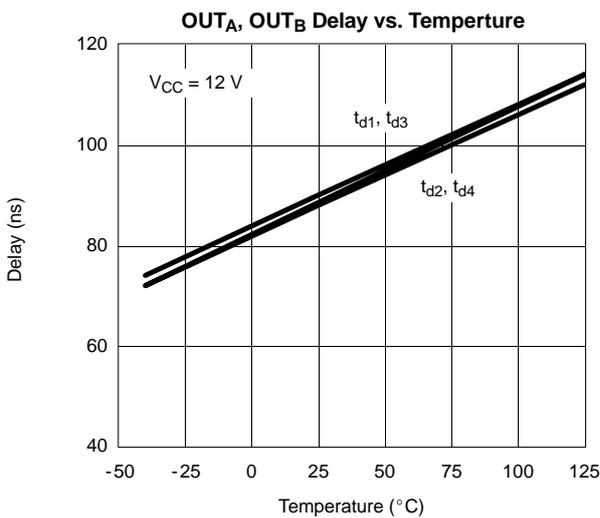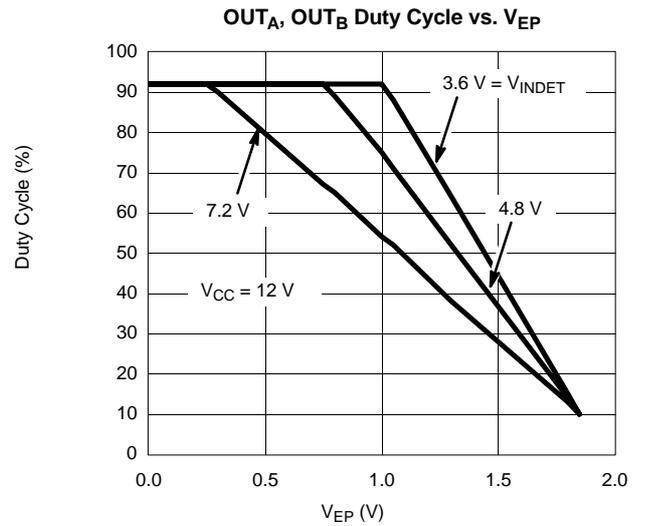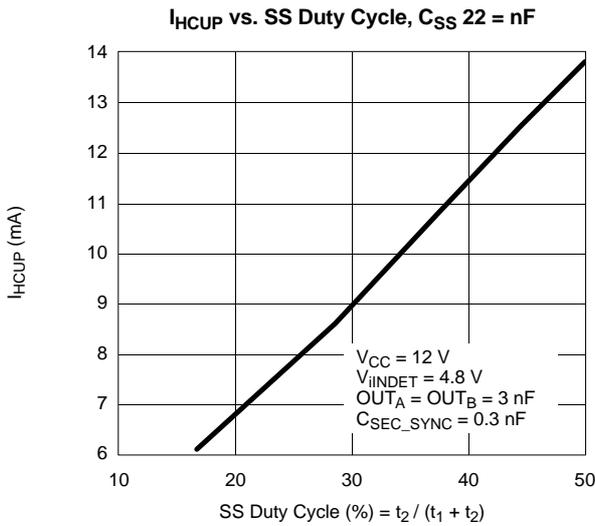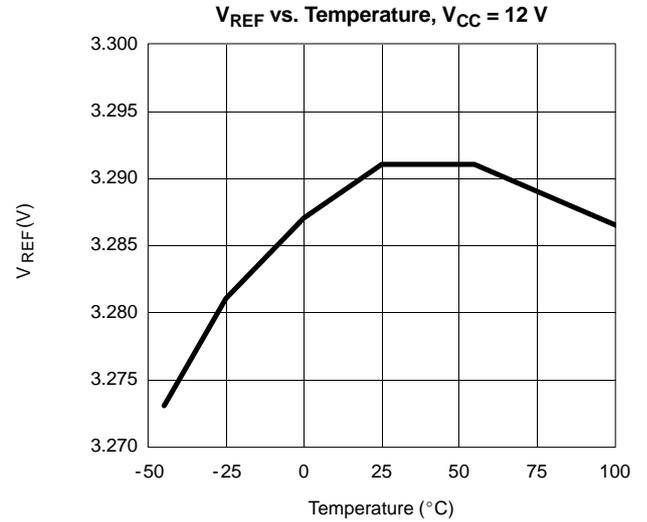
TYPICAL CHARACTERISTICS

I_{REG2} vs. Temperature

Drivers w/o C_{LOAD}
V_{IN} = 48 V

I_{CC3} + I_{CC5} vs. Temperature

Drivers w/o C_{LOAD}
V_{CC} = 12 V
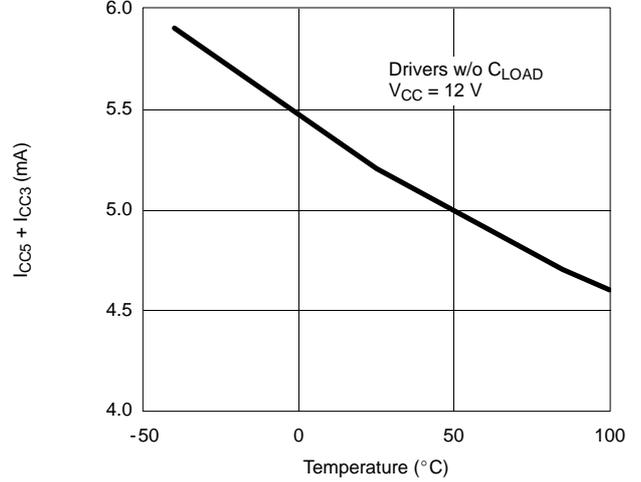
OUT_A, OUT_B I_{SOURCE} vs. V_{OH}

V_{CC} = 12 V
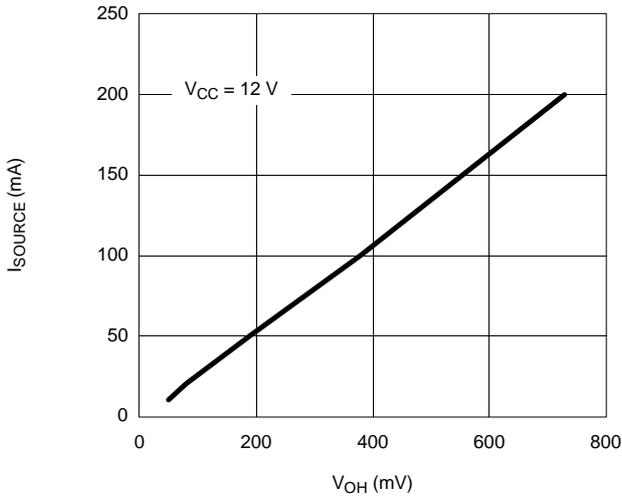
OUT_A, OUT_B I_{SINK} vs. V_{OL}

V_{CC} = 12 V
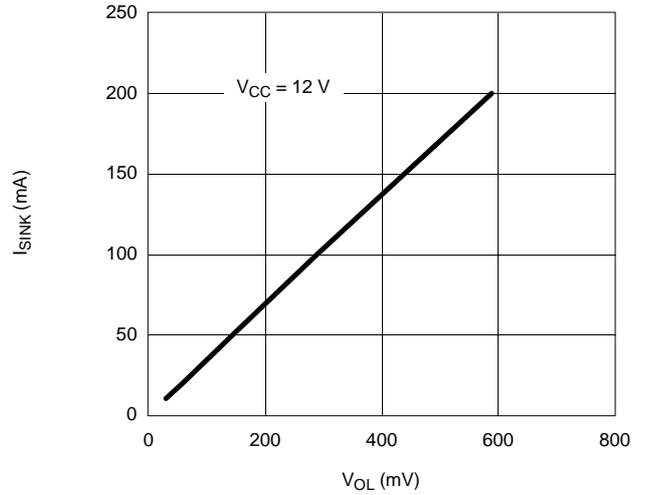
SEC_SYNC I_{SOURCE} vs. V_{OH}

V_{CC} = 12 V
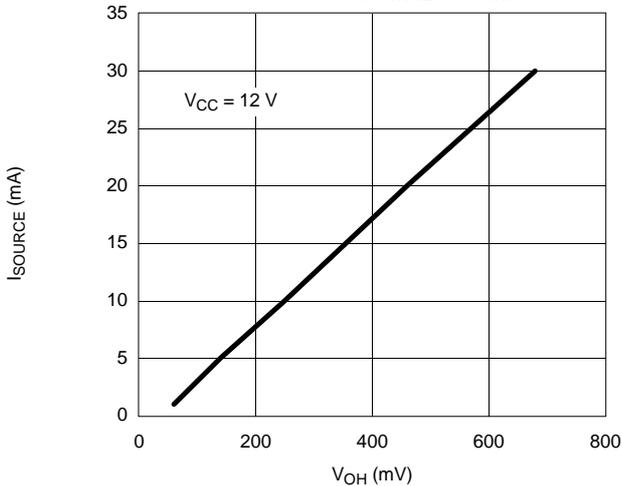
SEC_SYNC I_{SINK} vs. V_{OL}

V_{CC} = 12 V
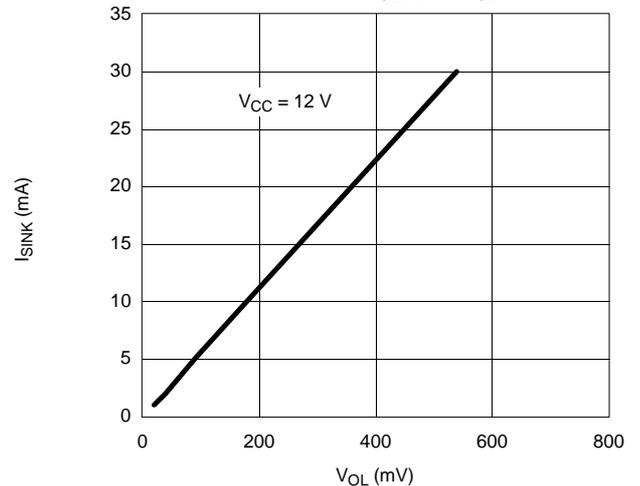
TYPICAL WAVEFORMS

Figure 8. Over Current Hiccup (CS2 = 200 mV)

OUT$_A$ 20 V/div

V$_{CC}$ = 12 V

OUT$_B$ 20 V/div

CS2 100 mV/div

GND

SS 1 V/div

C$_{SS}$ = 22 nF

200 μs/div
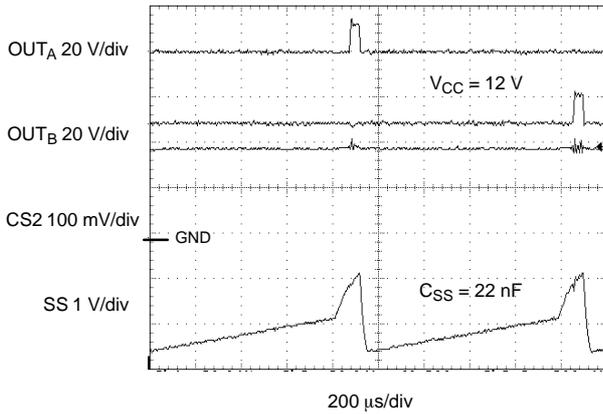
Figure 9. Over Current Hiccup Cycle

OUT$_A$ 20 V/div

V$_{CC}$ = 12 V

OUT$_B$ 20 V/div

CS2 100 mV/div

SS 1 V/div

C$_{SS}$ = 22 nF

200 μs/div
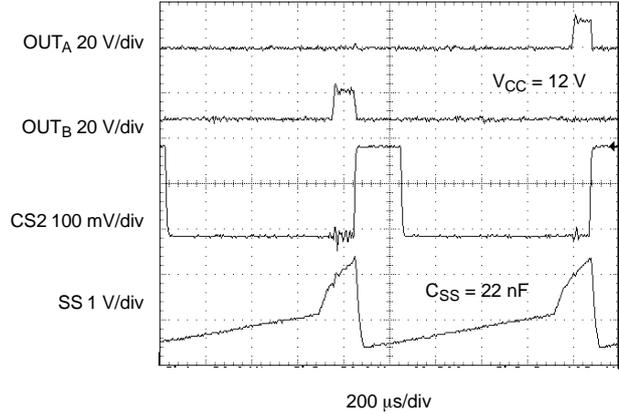
Figure 10. Pre-Regulator Start-Up

Δ: 0 s
@: 360μs

10 V/div

V$_{INEXT}$

V$_{CC}$

Ch1   10.0 V   Ch2   10.0 V   M2.00ms   Ch1   5.8 V

2 ms/div
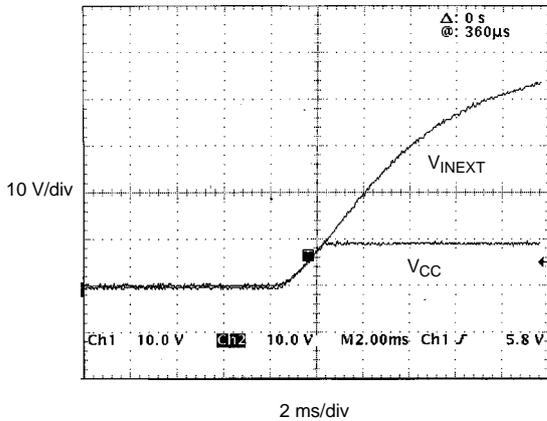
Figure 11. Operating Driver Waveforms

V$_{CC}$ = 12 V

OUT$_A$ 5 V/div

SEC_SYNC
5 V/div

OUT$_B$ 5 V/div

500 ns/div
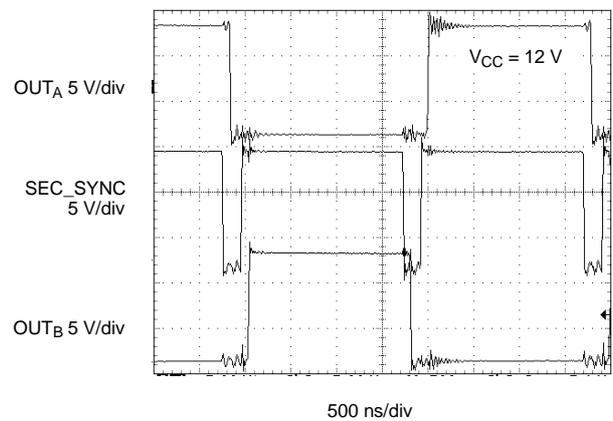
Figure 12. SEC_SYNC Set-Up Time (t$_{d3}$, t$_{d4}$)

V$_{CC}$ = 12 V

OUT$_A$ 5 V/div

SEC_SYNC
5 V/div

100 ns/div
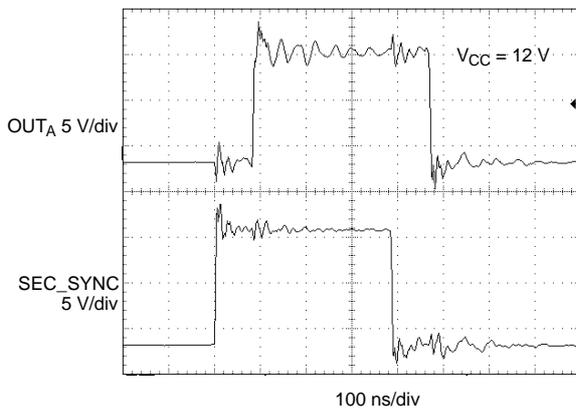
Figure 13. SEC_SYNC Set-Up Time (t$_{d1}$, t$_{d2}$)

SEC_SYNC
5 V/div

V$_{CC}$ = 12 V

OUT$_B$ 5 V/div

100 ns/div

New Product
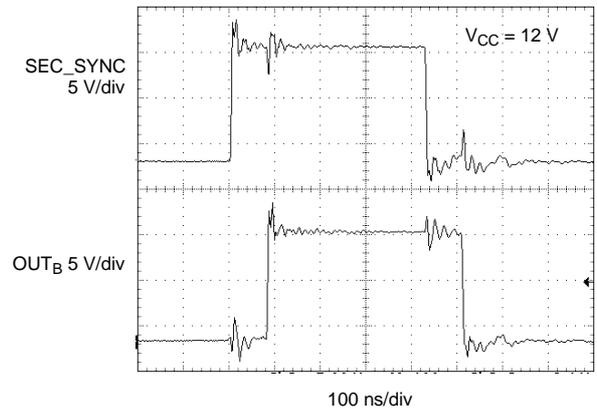
LOGIC REPRESENTATIVE APPLICATION SCHEMATIC

Figure 14.

Figure 15.